CPU-31/32 Reference Sheet

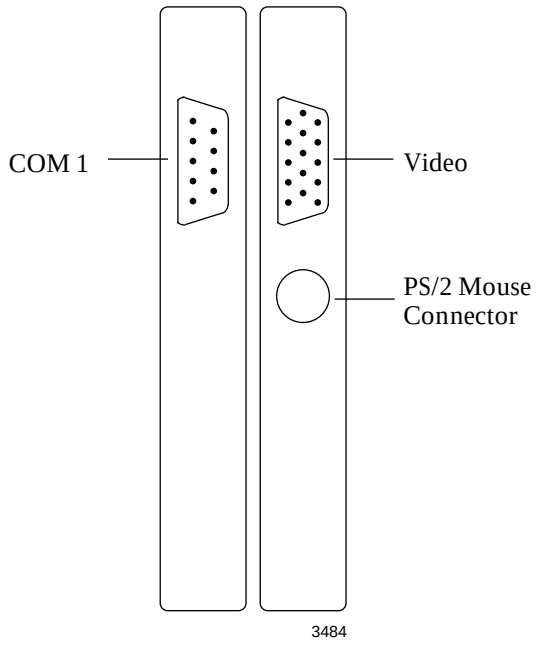

Figure 1: CPU 31/32 Backplate Connectors

CPU-31/32 Features Overview

- **Microprocessor**: Intel Pentium, 100 MHz
- **Cache**: The CPU-31/32's cache is implemented with synchronous SRAM. This feature enhances the operation of the circuit by eliminating wait states on cache accesses. The default cache size is 256 KB.
- **Intel Triton II Chipset**:
  - Flexible CPU interface including full write-back internal and external cache operation
  - Concurrent CPU/cache and PCI/DRAM operation
  - Synchronous Pipelined Burst SRAM cache
  - Extended Data Out as well as Fast Page Mode DRAM access
  - Parity or Error Correction Code support
  - Fully functional compliance of the PCI interface
  - Plug and Play capability
  - Power management
  - Supervisor utilities
  - Universal Serial Bus support
- **Video**: The CPU-31/32 is implemented with advanced video functions including the 65550 video chip from the Chips & Tech family. Features include:
  - 64-bit graphics engine
  - Video playback acceleration
  - 24-bit color video digital-to-analog converter
  - Hardware Windows acceleration
  - 32-bit PCI host interface
- **System Memory**:
  - Four vertical 72-pin SIMM sockets support DRAM memory configurations from 8 to 512 MB (8 MB default)
  - Uses standard 5V, 70ns/60ns single-sided or double-sided 72-pin SIMMS
- **Enhanced IDE Interface**: Enhanced IDE controller drives up to four IDE devices with transfer rates up to 22 MB/s. The CPU-31/32 includes two separate IDE data bus and control signals.
- **SCSI Interface:** This interface is implemented with a PCI Ultra SCSI controller.