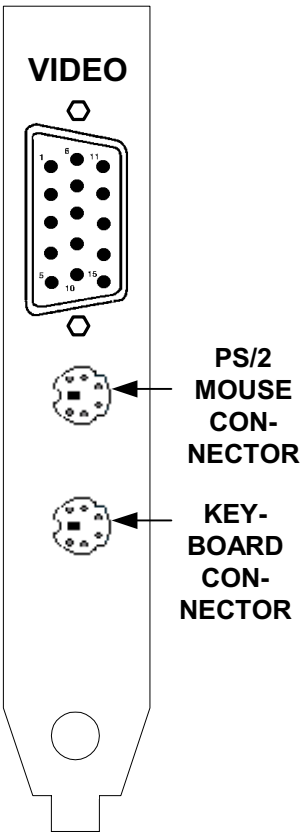
CPU-33 Backplate Connectors



NOTE:
This reference sheet is provided to illustrate the layout of the CPU-33 back plate installed in the FW1100/1150 and Sm@rtRouter 3100/3150 unit's back panel diagrams shown in the Hardware Installation Guides.

CPU-33 Features Overview

- MICROPROCESSOR SUPPORTED: (maximum internal CPU clock speed): Intel Pentium: 233MHz

- CACHE: The CPU-33's cache is implemented with synchronous SRAM. This feature enhances the operation of the circuit by eliminating wait states on cache accesses. Cache size is 256KB (default)

- INTEL TRITON II CHIPSET:
  - Flexible CPU interface including full write-back internal and external cache operation.
  - Concurrent CPU/cache and PCI/DRAM operation.
  - Synchronous Pipelined Burst SRAM cache
  - EDO as well as Fast Page Mode DRAM access.
  - Parity or ECC Support
  - Full functional compliance of the PCI interface.
  - PnP capability
  - Power management.
  - Supervisor Utilities
  - USB Support
- **VIDEO:** The CPU-33 is implemented with advanced video functions including the C&T 65550 video chip from the Chps & Tech family. Its features include:
  - 64-bit graphics engine
  - Video playback acceleration
  - 24-bit color video DAC
  - Hardware Windows acceleration
  - 32-bit PCI host interface

- **SYSTEM MEMORY:**
  - Four vertical 72-pin SIMM sockets support DRAM memory configurations from 8 to 512MB (8MB default).
  - Uses standard 5V, 70ns/60ns single-sided or double-sided 72-pin SIMMS

- **ENHANCED IDE INTERFACE**: Enhance IDE controller can drive up to four IDE devices with transfer rates up to 22MB/s. The CPU-33 includes two separate IDE data bus and control signals.

- **SCSI INTERFACE**: This interface is implemented with a PCI Ultra SCSI controller. The circuit uses a Symbios 53C860 controller to perform this function.