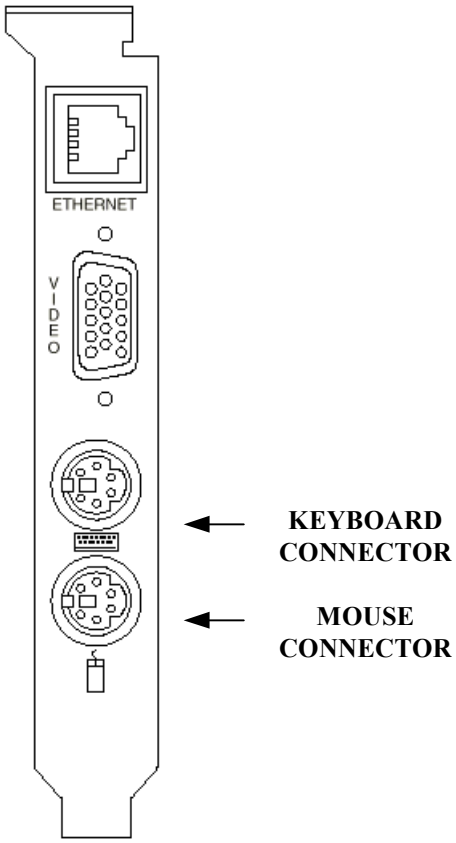
CPU-39 Backplate Connectors



NOTE:
This reference sheet illustrates the layout of the CPU-39 backplate installed in the Freeway 1200/1300 and Sm@rtRouter 3200/7200 units as described in the Freeway and Sm@rtRouter Hardware Installation Guides.

CPU-39 Features Overview

- **MICROPROCESSOR SUPPORTED:** 233 MHz Intel Pentium Processor
- **CACHE:** The CPU-39's cache is implemented with synchronous SRAM. This feature enhances the operation of the circuit by eliminating wait states on cache accesses. Cache size is 512 KB.
- **INTEL TRITON II CHIPSET:**
  - Flexible CPU interface with Level 2 write-back internal and external cache operation
  - Synchronous Pipelined Burst SRAM cache
  - Up to 512 MB EDO memory
  - Parity or ECC support
  - Full functional compliance of the PCI interface
  - PCI SVGA and 10/100 Mbit Ethernet
  - Power management
  - Supervisor utilities
  - USB support
- **CLOCK/CALENDAR:** Real-time clock with (replaceable) battery backup, includes 256 byte CMOS
- **SYSTEM MEMORY:**
  - Two banks of two 72-pin latching SIMM sockets
  - Up to 512 MB Extended Data Out, 60 ns
- **INTERFACES:** Supports Bus master PCI-EIDE and floppy drive
- **RELIABILITY FEATURES:** Filtered serial connectors, keyboard voltage protected by self-resetting fuses. Board serial number in EPROM.