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ICP2432B
Hardware Description and Theory of Operation

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ICP2432B Hardware Description and Theory of Operation

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Preface

Purpose of Document

This manual describes Simpact's ICP2432B front-end communications processor, its architecture, and how it works in an PCI bus system.

Intended Audience

This document should be read by maintenance technicians, computer system integrators, and software developers who need detailed information about the operating theory and features of the ICP2432B hardware.

Required Equipment

The ICP2432B board mounts in any full PCI bus slot that supports bus mastering.

Organization of Document

If you are not familiar with Simpact's front-end communications processors, you should read Chapter 1 and Chapter 2. If you are familiar with front-end communications processors, you may wish to skip these overviews and go directly to the detailed technical descriptions in Chapter 3.

Chapter 1 contains a functional overview of the ICP2432B.

Chapter 2 describes the basic operation of the ICP2432B in a system.

Chapter 3 contains a detailed theory of operation with hardware descriptions.

References

ColdFire® Family Programmer's Reference Manual, CFPRM/D, Motorola, Inc.

MCF5407 ColdFire® Integrated Processor User's Manual, MCF5407UM/D, Motorola Inc.

PCI 9054Data Book, PLX Technology

Z16C30/Z16C32 IUSC User's Manual, Zilog, Inc.

Document Conventions

The following conventions apply throughout this document:

- A signal name that appears with an overline, for example, $\overline{\texttt{ZAS}}$, indicates that the signal is asserted low true.
- "Communications bus" is equivalent to "Z-BUS."
- Bits are numbered from right to left, beginning with zero. Bit zero is the low-order bit.

Revision History

The revision history of the *ICP2432B Hardware Description and Theory of Operation*, Protogate document DC900-2006, is recorded below:

Document Revision	Release Date	Description
DC 900-1501A	May, 2002	Prelimary release

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Chapter

1 ICP2432B Overview

The ICP2432B intelligent communications processor is an ancillary computer dedicated to the processing of communications-related data.

The ICP2432B hardware is a single-board computer with central processing unit (CPU), synchronous dynamic random access memory (SDRAM), programmable read-only memory (PROM), and input/output (I/O) circuitry. The software consists of an onboard operating system, diagnostic tests, host interface drivers, and application routines.

1.1 Purpose of the ICP2432B

The main purpose of the ICP2432B is to improve the overall computing efficiency of the host computer. To do this, low-level communications tasks traditionally performed by the host central processor are migrated to the ICP.

An ICP increases overall system bandwidth by distributing the I/O processing away from the host CPU. In the traditional minicomputer or microcomputer architecture, the host services all I/O requests. This load on the CPU has grown steadily as computer peripherals have become increasingly more powerful. Modern operating systems allow intelligent front-end processors to perform these relatively simple tasks. The result is an overall increase in system throughput.

Table 1–1 sums up the attributes of the ICP.

Table 1–1: ICP Hardware Features and Benefits

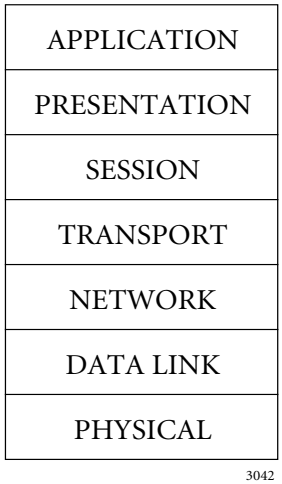
Features	Benefits
MCF 5407 integrated processor	4-gigabyte linear address space Allows use of familiar, powerful program development tools (assemblers, C compiler, editors) Integrated DMA support for PCI transfers
PLX 9054PCI interface	32-bit master/slave interface PCI revision 2.2 compliant
Large RAM memory	Space for application tasks and real-time executive Applications are downloaded from the host rather than from ROM to make it easier to update software
Individually programmable ports	One ICP services lines with different characteristics such as parity, data rate, synchronous *vs.* asynchronous, CRC checking Full modem support Flexibility in changing environments
DMA-controlled data transfer	Full duplex support for high-speed applications
Multiple electrical interfaces	Supports EIA-232 (V.28), EIA-422 (V.11), EIA-449, EIA-530, MIL-STD-188C, MIL-STD-188-114A Balanced Type II, and V.35
Single-module form factor	Easy mounting in standard backplane

1.2 ICP2432B Applications

The ICP2432B is a general-purpose computer that can do many different tasks. At system startup, the ICP2432B gains its run-time personality from downloaded application software. The application software may be customer-specific or part of an ICP2432B turnkey product.

Communications software systems that use the ICP2432B can fit the International Standards Organization (ISO) open system interconnection (OSI) seven-layer reference model for communications protocols. Figure 1–1 shows this model. In most cases the ICP is programmed to perform up to the first three levels of this model.

Once the software download has been completed, the ICP2432B hardware and software combination performs its assigned task until a board-level reset initiates another startup sequence.



	Layer Number	Function
APPLICATION	7	Services applications
PRESENTATION	6	Code conversion, data format
SESSION	5	Coordinates interaction between applications
TRANSPORT	4	End-to-end data integrity
NETWORK	3	Routes information
DATA LINK	2	Exchanges data with physical link
PHYSICAL	1	Transmits/receives bit stream to medium

Figure 1–1: ISO OSI Reference Model

Chapter

2 System Operations

This chapter describes the ICP2432B hardware and its operation in host systems.

2.1 ICP2432B Architecture Overview

The ICP2432B computer uses a primary bus for the CPU,the memory, and the PCI host interface, and the Glue Logic support device. The secondary bus is the Z-Bus on which resides the IUSC serial controllers and the Sipex electrical interface chips on the 2 and 4 port configurations.

2.2 General Operation

Operation of the ICP2432B occurs in two phases: startup and routine operation. When power is initially applied to the ICP2432B, its CPU begins execution at a memory address in the PROM device. This location contains instructions to set up the basic working environment for the CPU.

2.2.1 Startup

Startup begins with the execution of diagnostic firmware that tests the major sections of the ICP2432B hardware. Upon successful completion of these tests, the host interface is initialized and the host downloads the ICP's operating system and application program software, through the PCI bus interface circuits, into the ICP memory. After these programs have been downloaded, the CPU begins to execute the downloaded software.

2.2.2 Routine Operation

During routine operation, the ICP2432B does all the communications-related work. The software program downloaded during startup is used to operate the general-purpose ICP2432B communications hardware in the mode required by the host system. This program is typically an implementation of some special purpose communications protocol such as X.25, SDLC, or ADCCP.

The ICP2432B remains in the routine phase of operation until a board reset is issued by the host software, the host-bus hardware, or the reset button.

2.2.3 Reset

A hardware reset causes the ICP2432B to stop execution of program instructions. No attempt is made to save the current state of the CPU operation. The hardware reset causes the CPU to go back to the startup phase.

2.3 Operation in the Application Environment

The ICP2432B offloads the host, thus increasing overall system performance. Traditionally, the host's CPU executes the tasks related to the operation of serial communications. These tasks can be extensive, and many require processing in real time. The ICP2432B hardware, combined with application software, is capable of executing many of these protocol-dependent, low-level tasks. The ICP2432B receives the application software download from the host system during the system startup phase.

2.3.1 Communications Traffic

When the software download is complete, communications traffic is accepted and processed for transfer to or from the host. In most applications, the data format used by the host processor is very different from the format transmitted on the serial communications links. Many additional structures must be added to the raw data processed by the host system in order to detect errors, retransmit frames, and maintain data integrity at

the data link level. The software programs downloaded into the ICP2432B perform these tasks.

2.3.2 Ports

The ICP2432B is equipped with two, four, or eight high-performance serial communications ports. The ICP2432B, when combined with the appropriate distribution cables and/or adapters, can support such electrical interface specifications as EIA-232 (V.28), EIA-449, EIA-530, MIL-STD-188C, MIL-STD-188-114A Balanced Type II, and V.35.

Chapter

3 Hardware Survey

This chapter describes the ICP2432B architecture, memory map, buses, and devices. Refer to the block diagram of the board, Figure 3–1, throughout the chapter.

3.1 Architecture

The ICP2432B is a single-board computer designed to optimize communications processing for systems with PCI bus support.

3.1.1 Bus Architecture

As shown in Figure 3–1, the ICP2432B has a primary bus on which the CPU, PROM, SDRAM, PCI interface, and the interface to the communications bus, the Z_Bus. The primary bus is a non-multiplexed bus architecture that has a 32 bit wide address bus and a 32 bit data bus. The communications bus is implemented as a Zilog 16 bit wide multiplexed bus (Z-BUS) that provides 32 bits of address space adn a 16 bit wide data path.

3.1.2 Host Interface

In most cases, the host machine is the ultimate source or destination of the data being transmitted and received through the serial communications devices. The board requires a mechanism for issuing commands, determining status, and controlling data exchange with the host system in which it resides.

The ICP2432B PCI provides both a 32-bit PCI bus master and bus slave “end point” device (not a bridge). It is a 33Mhz, +5v interface compliant with Rev 2.2 of the PCI Local Bus Specification.

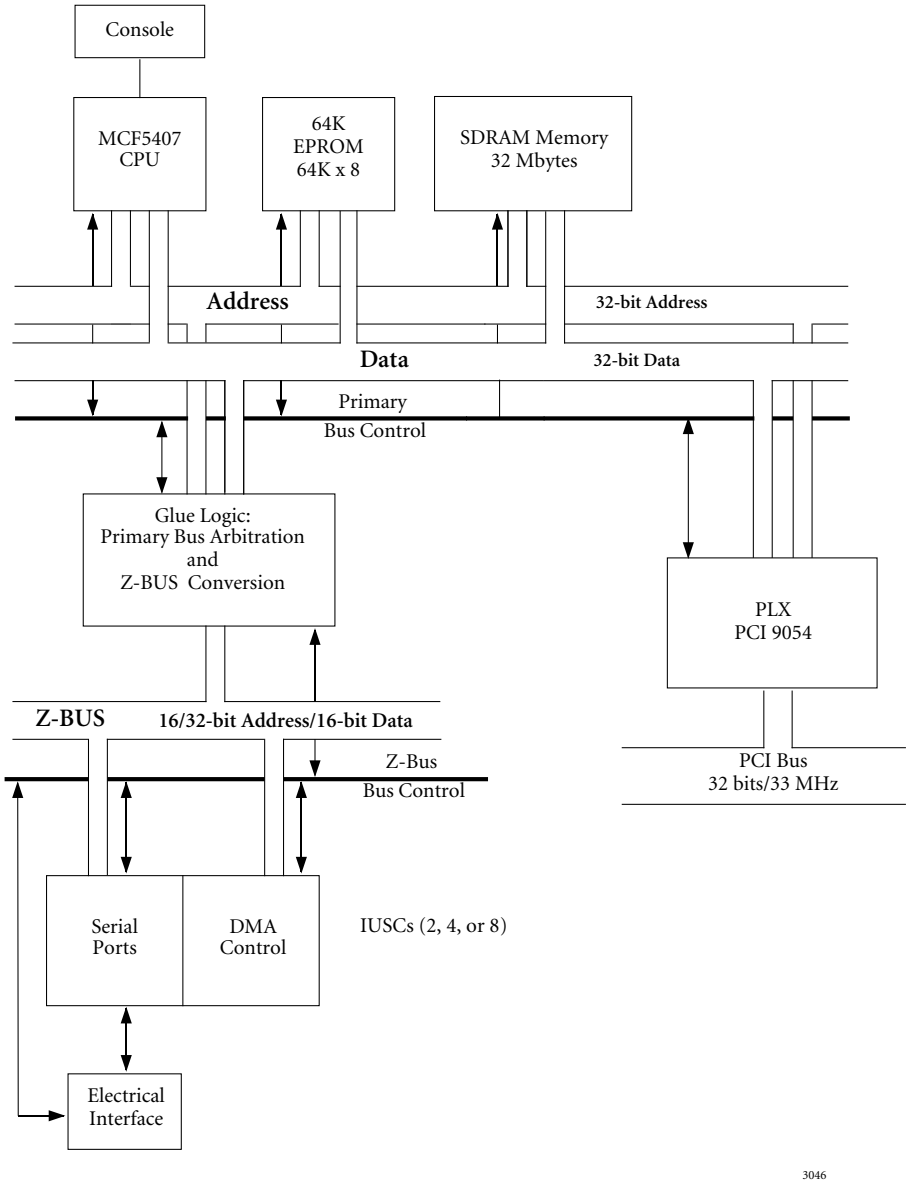


Figure 3–1: ICP2432B Block Diagram

The interface comprises multiple mailbox registers and dual FIFOs. The PLX 9054 has two integrated DMA controllers for transporting data between the host and the ICP. As a bus master (initiator) it supports Memory read and Memory write commands. As a slave (target) is supports memory and I/O Reads/Writes as well as Configuration Reads/Writes.

The mailboxes are used to pass messages between the ICP and the host to coordinate data exchange while the FIFOs are used for actual data transfer. The 9054 has 2 "door-bell" registers which are used to generate interrupts to the host and the ICP. See Section 3.5 on page 37 for details.

3.2 Memory Map

The ICP2432B memory map, shown in Figure 3–2, is divided into nine address ranges: non-volatile (EPROM) memory space, glue logic space, PLX 9054 access space, the CPU's internal peripheral space, the CPU's internal static RAM, volatile SDRAM memory space, Z-BUS space, an usnassigned space, and a space reserved for direct CPU access to PCI memory.

3.2.1 Non-volatile Memory

The 256-megabyte space beginning at address 0000_0000 hex is the non-volatile memory space. The ICP2432B FLASH occupies the lowest 64 kilobytes. The additional space is reserved for future expansion.

3.2.2 Glue Logic Space

The 256-megabyte space beginning at address 1000_0000 hex is the Xilinx glue logic device space. The direcct acccess is primarily for bus status and access to a one mega-hertz 32 bit wide clock register.

3.2.3 PLX 9054 Access Space

In this 256 megabyte space, beginning at 2000_0000, the CPU accesses the PLX 9054 PCI interface device (see Section 3.3.5 on page 33).

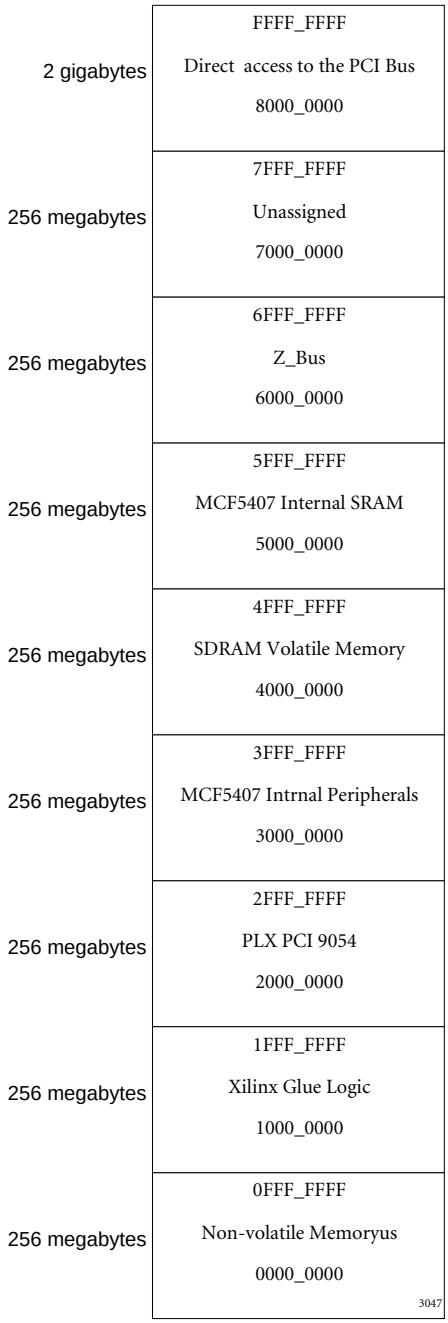


Figure 3–2: ICP2432B Memory Map

3.2.4 CPU's Internal Peripheral Devices

The 256 megabyte space, beginning at 3000_0000, is for the various internal peripherals of the ColdFIre MCF5407. These devices include the real time clock and the console serial interface.

3.2.5 Volatile SDRAM Memory

The 256 megabyte space beginning at address 4000_0000 hex is for the 32 megabytes of Synchronous Dynamic Random Access Memeory (SDRAM) volatile memory space.

3.2.6 Static RAM Memory

The 256 megabyte space beginning at address 5000_0000 hex is for the 4 kilobytes of Static Random Access Memeory (SRAM) which is interanl to the CPU.

3.2.7 Z-BUS Space

The 256 megabyte space beginning at address 6000_0000 hex is the Z-BUS space. To simplify address decoding logic, each device is assigned a four-kilobyte window. These devices are the integrated universal serial controllers (IUSCs) with integral DMA controllers (Section 3.4.2), the mode control registers for the Sipex electrical interface devices (Section 3.4.3), the input register for the Test Mode inputs (Section 3.4.4), and the board ID register. The additional space is reserved for future mezzanine board products.

3.2.7.1 Reserved Space

The 256 megabyte space beginning at 7000_0000 hex is currently unassigned and is reserved for expansion.

3.2.7.2 Direct CPU Access to PCI memory

The two gigabyte space beginning at 8000_0000 hex is reserved for direct access to PCI memory space by the CPU.

3.3 Primary Bus

The ICP2432B primary bus provides the addressing and data path between the CPU, the SDRAM, the FLASH(EPROM), the PCI interface device, and the glue logic (the support circuitry required for timing and control of the buses). Descriptions of the major devices, glue logic, bus signals, and operation of the primary bus are contained in this section. For clarity, the processor description precedes the descriptions of the bus operation and other devices that connect to this bus.

3.3.1 ColdFire® MCF5407 Integrated Processor

The MCF5407 processor is a highly integrated device that provides extremely flexible configurations and includes the following major functional blocks.

- Core Processor
- Instruction and Data Caches
- Internal Static RAM
- System Integration Module (SIM)

3.3.1.1 Core Processor

The processing power for the MCF5407 is provided by its core central processing unit. This core delivers a subset of the Motorola 68K processor family. The core has been optimized for producibilty and speed. Internally the 5407 has a Harvared architecture memory which operates in concert wtih the instruction and data caches as well as the two banks of internal static RAM. The core runs at 160 megahertz, 4 times the external clock of 40 megahertz.

3.3.1.2 The Caches

The instruction cache is 16 kilobytes and the data cache is 8 kilobytes. Both are 4 way set associative. These caches run at the core's clock speed.

3.3.1.3 Internal Static RAM

The statis RAM is confiured as two blocks of 2 kilobytes each. These blocks can be attached to either the instruction bus or the data bus independently. The blocks provide single cycle access at the core's clock speed.

3.3.1.4 System Integration Module, the On-chip Peripherals

The on-chip peripherals described below are independent modules. An inter-module bus (IMB) is used for all on-chip communications. The IMB is similar to a traditional external bus with address, data, clock, interrupt, arbitration, and handshake signals. The IMB ensures that communication between the modules is fully synchronized and that arbitration and interrupts can be handled in parallel with data transfers.

Direct Memory Access Module

The MCF5407 contains 2 high-speed 32-bit DMA controllers. Each DMA controller consists of two independent programmable channels. Each channel has separate request, acknowledge, and done signals. Each channel can operate in flyby or dual address mode and supports byte, word, and longword transfers. It supports both burst and cycle steal external request modes. The DMA controller can be configured to release the bus back to the CPU when a high-priority interrupt occurs. The CPU32+ and the DMA controller arbitrate for the bus in parallel with executing bus cycles, typically eliminating all bus arbitration overhead and allowing DMA and CPU bus cycles to occur back-to-back without intervening idle clocks.

Serial Module

The MCF5407 contains two highly configurable full-duplex UARTs. The second UART can provide soft modem support

The ICP2432B uses serial channel 1, configured as a 9600 baud asynchronous port, as a console to provide command and status input /output to software development and manufacturing test personnel.

The channel A RTS and CTS pins are used by diagnostic code to determine mode of operation. Manufacturing loopback connectors tie RTSA to CTSA to signify that full manufacturing diagnostics are to be executed.

UART 2 is has only Transmit and Receive dat leads brought out to its own 10 pin header. This port has been earmarked to function as a printer port or as a SingleStep monitor port.

Both channels have a ten pin header mapped for mass termination to a standard DB9 connector.

System Integration Module (SIM)

The SIM provides the external bus interface for both the CPU32+ and the DMA modules. It also provides programmable circuits to perform address decoding, chip selects, wait-state insertion, interrupt handling, clock generation, bus arbitration, watchdog timing, discrete I/O, and power-on reset timing.

The internal registers for all of the modules are contained in a single 4 kilobyte block that is relocatable along 4 kilobyte boundaries.

3.3.1.5 MCF5407 Power-up Defaults

At power-up/reset time, the MCF5407 registers and the external pins they control are reset to default conditions. The functionality of these pins are configurable and, since external devices and logic are connected to them, unique to each hardware design. A method is required to enable the MCF5407's first fetches from ROM to operate properly before these SIM control registers are initialized.

The MCF5407 samples bits 7:0 of the data bus on the rising edge of RESET for the design dependent power-up configuration. The initial configuration is for a 32 bit wide address bus, a 4x clock multiplier for the MCF5407's core.

3.3.1.6 System Configuration and Protection

After initial power-up, the system configuration is determined by initializing the MCR and AVR registers. These registers control the port pin functions, the debug support, the interrupt arbitration of on chip modules, and the external interrupts that require auto-vector support.

The ICP2432B is configured as follows:

Module Base = 3000_0000, **Parallel Port + 0x248**

Bit #	Direction	Usage
7	in	(not used)
6	in	(not used)
5	in	(not used)
4	in	(not used)
3	in	(not used)
2	in	(not used)
1	out	a zero drives the green LED on
0	out	a zero drives the red LED on

3.3.2 CPU

For complete information on the MCF5407, see Motorola's *MCF5407 ColdFire®Integrated Microprocessor User's Manual.*

3.3.3 SDRAM

The DRAM memory is the ICP2432B's central resource and is used for both executable code and protocol data buffers. The memory can be accessed by the MCF5407's CPU and DMA controller and by the integrated DMA controller within each of the IUSCs. The Glue Logic provides all of the arbitration for this central memory resource and the primary bus in general. The MCF5407 is nominally always granted the bus. The arbitration logic will remove the grant if any of the IUSCs on the Z-Bus or the PLX PCI interface need the bus. The priority, from highest to lowest, is external bus masters

(IUSCs), PCI controller, and MCF5407.

The memory system is implemented as a 32-bit, Synchrounous DRAM memory system that supports byte, word, and longword access. Most of he memory control logic is provided by the SDRAM controller of the MCF5407. The Glue Logic takes care of the address muliplexing required by the SDRAM chips.

3.3.4 Non-volatile Memory (FLASH)

The ICP2432B-PCI requires firmware to execute manufacturing diagnostics, power-up self tests and the bootload code that coordinates the download of OS/Protogate and protocol images from the host.

The ICP2432B provides a 32-pin PLCC socket for a non-volatile device. The socket supports any 512kb-to-4Mb (64k-to-512k byte) EPROM/FLASH/OTP device whose footprint meets the JEDEC standard. Since the firmware code is seldom changed, in-circuit write cycles for FLASH or E2PROM devices is not supported. A 512 kilobit (64 kilobyte) device is standard at this time.

3.3.4.1 Diagnostics

Self-test diagnostics are executed on initial power-up. These tests validate the control circuitry, memory, processor and Z-BUS peripheral devices, interrupt operation, and bus error logic of the ICP2432B hardware. Test status and error reporting may be monitored by connecting a terminal to the console port of the ICP.

The successful completion of the diagnostics allows the downloader to execute on request from the host.

Additional diagnostics are run if:

- the RTS modem signal of the ICP2432B console port's drives its CTS input signal, or

- the CTS signal is driven by a console device's DTR and it is "true" and the console device responds with a "P" (P for production) in response to an ENQ.

The production diagnostics include IUSC DMA tests and IUSC/Sipex digital I/O loop back tests. These tests are not run in real environments because the data and control signals will not respond predictably without self-port loopback connectors installed.

If the console device responds with a "D" (D for debug), the PROM code calls the memory/device display routine (Peeker) so that a programmer can examine various memory locations and device registers that may not have been changed by the reset.

Note that most program debugging should be done with a symbolic debugger such as `SingleStep` which can access the MCF5407 through its Background Debugging Mode port, a 266 pin header on the ICP.

3.3.4.2 Downloader

The CPU uses the boot loader code and the host driver to download the OS/Protogate executive and applications from the host to the board. The ICP2432B does this by moving the executable images to the onboard memory as a bus master on the PCI bus. The CPU begins execution of the downloaded code at the completion of the download sequence.

3.3.5 PCI Interface Device

The processor bus also includes the PCI interface device. This device is a PLX 9054. The device has six FIFOs, bi-directional mailboxes, and programmable interrupt controls (Doorbells). The device is accessed at 2000_0000 hex. For more information on the PLX 9054, refer to PLX's *PCI 9054 Data Book*.

3.3.6 Debug Support

The ICP2432B implements the BDM debug support via a 26 pin header. Debugging can also be done via the Console or serial Printer port with SingleSteps monitor which can be down loaded with OS/Protogate and the reqisite protocol software.

There arre also two surface mount puhbuttons oon teh ICP. The lower one ir a Reset button and the upper one is an Non Maskable Interrupt (NMI) button.

The ICP2432B base board has a 10-position box-header located on the upper edge of the PCB. This header is easily accessible and is the console port. Just below the console port header is the serial printer port. A thrid 10 pin header is provided for acces to the Glue Logic chip, a Xilinx Spartan-XL device.. Below thse is the 26 pin BDM port header.

3.4 Communications Bus (Z-BUS)

The ICP2432B communications bus exists as a space in the CPU memory map and is composed of integrated universal serial controllers (IUSCs), electrical interface control registers, a modem Test Mode input register, a board ID register, and the support circuitry required for timing, data transfer, bus arbitration, and interrupt operations. This section gives a full description of the major devices, support circuitry, bus signals, and operation of the communications bus. The communications bus is implemented as a Zilog multiplexed bus and is referred to as the Z-BUS throughout this section.

3.4.1 Z-BUS Operation

The Z-BUS is a time-multiplexed bus made up of 16 address/data lines and 13 miscellaneous control lines. The possible bus masters on the Z-BUS are the MCF5407 and the four IUSC DMA controllers.

Each IUSC DMA controller has a separate bus request and acknowledge connection to an arbitration controller in the Glue Logic. This controller monitors these $\overline{\texttt{BUSREQ}}$ signals and grants the bus to one of the IUSCs by generating its $\overline{\texttt{BUSACK}}$ signal. CPU read, write, and interrupt transactions in the Z-BUS space require a Z-BUS conversion state machine to control address and data buffers for bus multiplexing, and to generate (using the Motorola signals) control signals that conform to the Z-BUS specification. This state machine also controls bus isolation between the Z-BUS and the processor bus.

3.4.2 Communication Devices with Integral DMA

The ICP2432B uses two, four, or eight Z16C32 integrated universal serial controllers (IUSCs) with integral DMA. Each IUSC is a single-channel, multi-protocol data-communications device that functions as a serial-to-parallel and parallel-to-serial data converter. It may be software-configured to satisfy a wide variety of serial communications applications. Each IUSC may be programmed to handle asynchronous formats, synchronous byte-oriented protocols such as IBM bisynchronous, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. The IUSC can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. Each IUSC includes modem control signals, data clock generation, vector-includes-status interrupts, and an integral DMA interface.

The transmitters and receivers of each IUSC have a 32-byte FIFO that can be loaded or emptied by byte or by word. The ICP2432B also has a nominal baud clock source of 3.6864 megahertz, plus a socket for an optional oscillator for specific, non-standard bit clocks.

The integral DMA controllers in the IUSCs can operate in any of four modes: Single Buffer, Pipelined, Array, and Linked List. Command and status information can be extracted or put into the lists of the last two modes. This feature allows automated reception of back-to-back frames of SDLC data without loss of data or frame rejection even at a 10 megabit per second rate. As with the serial controller sections of the IUSCs, the DMA controller sections can generate interrupts with Vector Includes Status which enhances interrupt response. Up to 64 kilobytes may be sent or received in one block out of or into multiple buffers.

3.4.3 Sipex Mode Select Register

The two- and four-port versions of the ICP2432B uses Sipex's SP506s which allows the software to select the electrical interface to be used while communicating with a modem or other device. The electrical interfaces are:

- EIA-232 (V.28)

- EIA-422 (V.11 and X.27)
- EIA-449
- EIA-530
- MIL-STD-188C
- MIL-STD-188-114A Balanced Type II
- V.35

The EIA-422 has two modes, one with termination resistors and one without. The other balanced modes have their termination resistors enabled all of the time.

An adapter is available that transitions from a standard DB25 to the V.35 block connector.

3.4.4 Test Mode Input Register

All modem control signals except Test Mode are handled directly by each port's IUSC. The Test Mode input status for all ports is accessible by the MCF5407 via the Test Mode register located at 6001_0000 hex on the Z-BUS. See Figure 3–3.

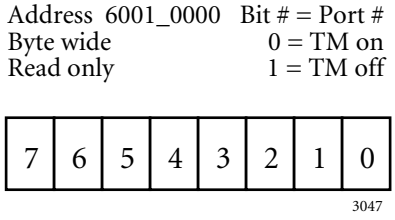


Figure 3–3: Test Mode Register

3.4.5 Circuits

Table 3–1 lists the complete set of circuits provided by the ICP2432B platform for each port. Some interfaces may only support a subset of these circuits. The EIA and MIL standards use unique names to identify some equivalent circuits. To simplify Simpact's design and production documentation, the ICP2432B uses a set of generic names for the interface circuits it supports.

Table 3–1: Interface Circuits

Transmit Circuits	
TD	Transmit data
TRXCO	Transmit clock out (ICP provides transmit clock)
RTS	Request to send
DTR	Data terminal ready
LPBKL	Local loopback
LPBKR	Remote loopback
Receive Circuits	
RD	Receive data
RTXC	Receive clock
TRXCI	Transmit clock in (modem provides transmit clock)
CTS	Clear to send
DCD	Data carrier detect
SYNC	Ring indicator
DSR	Data set ready
TM	Test mode

3.5 Host Interface

The ICP2432B front-end processor may be used with any computer that has PCI bus support.

3.5.1 Command and Status Registers

The ICP2432B has command and status registers (CSRs) that reside in I/O and memory space on the PCI bus. There are multiple registers in the PLX PCI 9054 used to control the operation of the device. Some of these are loaded from an serial EEPROM. The regisiters are broken up into groups: PCI Configuration, Local Configuration, Run Time, DMA, and Message Queue (for I2O support). Bits in the hardware registers allow the host to:

- Issue a reset to the ICP
- Control the master interrupt enable

3.6 Details of Operation

This section describes the interrupt, board timing, Z-BUS arbitration, reset, bus error, and NMI functions of the ICP2432B.

3.6.1 Interrupts

The ICP2432B implements the MCF5407 interrupt structure. The external interrupt level assignments are described in Section 3.6.1.1

3.6.1.1 Interrupt Structure

The ICP2432B uses three of the seven MCF5407 processor interrupt levels. Each interrupt source accesses its own interrupt request pin (INTRQn). These input pins are sampled by the processor. If any of them are asserted, and if the highest priority pin is greater than the current interrupt mask level, an interrupt request is made pending. The processor services the pending interrupt at the next instruction boundary. The MCF5407 supports both device-supplied vector (DSV) and autovector (AV) peripherals. The IUSCs are DSV, and the NMI and PLX PCI bus interface are AV. When the processor is ready to initiate interrupt servicing, it begins an interrupt acknowledge cycle. This cycle is similar to a normal read cycle. An $\overline{\text{IACK}}$ cycle at the pending interrupt level

enables the highest priority device at that level to present a vector byte. The processor uses this byte as an index to locate the peripheral's interrupt service entry point.

3.6.1.2 Interrupt Levels

The external interrupt levels can be summarized as follows:

Level 7	A non-maskable interrupt that causes the 68349 to stop execution of the current program and break to the debugging tool. NMIs may be issued by pushing the NMI push-button on the optional debug module
Level5	Used by the integrated universal serial controllers (IUSCs)
Level 3	Not used
Level 1	Used by the PLX PCI 9054

3.6.2 Timing

This section describes the clock generation logic of the ICP2432B and the transaction timings that result from its implementation.

3.6.2.1 Clock Generation

The ICP2432B uses synchronous state machine design techniques throughout the control logic to ensure accurate circuit performance and to increase circuit reliability. All clock signals are derived from a divider circuit that is clocked by the 40 MHz system oscillator.

The 40 MHz state clock is used by the CPU, the Z-BUS conversion, and arbitration state machines. A 2.5 MHz clock is used by the IUSC the IUSC DMA controllers and the Z-BUS interrupt state machine.

3.6.2.2 Transaction Timing

The advanced architecture of the MCF5407 makes exact instruction timing calculations difficult. The various pipelines and instruction FIFO buffer provide execution overlap capabilities, and the effects of operand misalignment complicate these calculations. Timing is also affected by memory system refreshes and Z-BUS arbitration delays. Refresh delays and PCI bus memory usage also affect IUSC DMA controller memory cycle times.

3.6.3 Z-BUS Arbitration

The MCF5407 and the two, four, or eight onboard IUSC DMA controllers may request use of the memory. The Z-conversion and the DMA arbitration state machines work together to determine which of these will be the next Z-BUS master.

3.6.3.1 Z-conversion State Machine

The Z-conversion state machine (inside the Glue Logic chip) enables, disables, and sets the direction of the CPU-to-Z-BUS address and data buffers, generates Z-BUS address and data strobes, and returns the $\overline{\text{TA}}$ signal to the processor support logic to indicate the end of the cycle.

3.6.3.2 DMA State Machine

On the 4 and 8 port mezzanines, DMA arbitration state machine monitors the request lines from each of the DMA devices and issues grant acknowledgments to them. This arbitration is round-robin.

Round-robin arbitration ensures that all DMA masters have equal access to the bus. It is implemented through the use of a circular pointer. The pointer scans the bus requests from the IUSC DMA controllers looking for an active request. If an IUSC DMA controller has a request asserted during its time slice, the pointer stops and the arbitration unit issues a bus grant to the requesting controller. After the DMA device completes its transactions and relinquishes mastership of the bus, the pointer starts scanning for the

next DMA controller with a bus request. This method ensures that, in turn, each DMA device is given a time slice to request use of the bus before the current master may reacquire the bus. This mode of operation is preferred for applications where all the ports are running at high data rates. Each DMA controller is guaranteed equal access to the bus bandwidth. This prevents data underruns and/or overruns on the serial communications lines caused by fixed priority schemes.

3.6.4 Reset

In normal operation, the reset controller keeps the $\overline{\text{RESET}}$ signal in a high-impedance state. This allows the MCF5407 to drive the line during the execution of a reset instruction. The reset controller PLD generates an 100 microsecond minimum reset pulse for the following conditions:

1. At power-up
2. When the PCI bus signal $\overline{\text{RST}}$ is asserted
3. When the reset switch is pushed

All of the devices, state machines, and configuration registers on the board are initialized to a known state when the $\overline{\text{RESET}}$ signal is driven low.

3.6.5 Non-maskable Interrupt (NMI)

The interrupt request controller issues a non-maskable interrupt (NMI) request when the NMI button is pressed. The MCF5407 executes the code pointed to by the AutoVector 7 vector. A hardware flag is posted in the Glue Logic that allows the CPU to determine the sopurce of the level 7 interrupt, either the NMI push button or a bus timeout.

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